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Total Pages  
(Including Cover Sheet): 4

Special instructions or supplemental message: **D/A1102 - REPLY BRIEF to follow.**

Inventor(s): Paul A. Hosier et al.

Group Art Unit: 2878

Application No.: 09/802,792

Filed: 3/8/2001

Examiner: Seung C. Sohn

Confirmation No.: 8347

**Title: COLOR FILTER CONFIGURATION FOR A SILICON WAFER TO BE DICED  
INTO PHOTSENSITIVE CHIPS**

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JAN 20 2004

**OFFICIAL****PATENT APPLICATION**  
**Attorney Docket No. D/A1102****IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Inventor(s): Paul A. Hosier et al.

Application No.: 09/802,792

Filed: 3/8/2001

Examiner: Seung C. Sohn

Confirmation No.: 8347

Art Unit: 2878

**Title: COLOR FILTER CONFIGURATION FOR A  
SILICON WAFER TO BE DICED INTO  
PHOTOSENSITIVE CHIPS****CERTIFICATE OF TRANSMISSION**

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Sir:

**REPLY BRIEF**

The following remarks are directed to remarks made by the Examiner in the  
Examiner's Answer of November 18, 2003.

Application No. 09/802,792

### **REMARKS**

To recapitulate briefly, the disclosure relates to a light-transmissive planar layer (such as of acrylic) placed on a silicon wafer prior to dicing of the wafer into chips. The wafer is diced with the planar layer still on it. The reference, Koizumi, also teaches placing a planar layer on the wafer; however, as is clearly taught in Koizumi, a portion of this planar layer must be removed before the wafer is diced into chips. In short, with the claimed invention, the entire planar layer *stays on* for the dicing step.

Independent claim 20 recites a wafer, including the planar layer thereon, suitable "for immediate dicing" into at least one chip. In the "Response to Argument" section of the Examiners' Answer, the phrase "suitable for immediate dicing" in claim 20 is queried as being ambiguous and confusing, i.e., "How early is immediate?"

For purposes of an *art* rejection, which is currently the issue under Appeal, the argument is irrelevant. The phrase is perfectly adequate to distinguish the invention from the cited reference. Figs. 11C and 11D of Koizumi do not show a wafer "suitable for immediate dicing" into a chip, as in independent claim 20: by the disclosure of Koizumi itself, the structure of Figs. 11C and 11D must go through *at least* the steps of Figs. 11E-F, which describe the *removal* of the planar layer before any dicing is contemplated. Koizumi simply does not teach a wafer having a planar layer in the groove which is, as claim 20 recites, "suitable for immediate dicing." Therefore, Koizumi does not anticipate the invention of claim 20.

Application No. 09/802,792

If the Examiner considers personal contact advantageous to the disposition of this case, please call Applicants' Attorney, Robert Hutter, at (585) 423-3811, Xerox Corporation, Rochester, New York 14644, or fax him at (585) 423-5240.

Respectfully submitted,



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January 20, 2004  
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